DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert M. McDermott on 1/26/2010.

The application has been amended as follows:

Please amend claim 1 as follows:

1(currently amended). An amplification circuit, comprising: an input to which an input voltage is provided, a capacitor arrangement, and a switching arrangement; wherein: the capacitor arrangement includes:

a first capacitor that is configured as a voltage-dependent capacitor having a first voltage-dependent capacitance, and

a second capacitor, coupled to the first capacitor, that is configured as a voltage-dependent capacitor having a second voltage-dependent capacitance;

the circuit is operable in two modes,

a first mode in which the input voltage is provided to an input terminal of at least the first capacitor, and

a second mode in which the switching arrangement causes charge to be redistributed between the first and second capacitors; and

the switching arrangement is configured to receive a first gain-control signal that is arranged to change the capacitance of the first capacitor and a second gain- control signal that is arranged to change the capacitance of the second capacitor; and

wherein the switching arrangement includes an input switch for selectively coupling the input voltage to the capacitor arrangement, and wherein in the first mode, the input switch couples the input voltage to the capacitor arrangement, and in the second mode, the input switch isolates the input voltage from the capacitor arrangement; and

wherein in the second mode, at least one of the first and second gain-control signals change a voltage on a gain-control terminal of the first and/or second capacitor.

Please cancel claims 2 and 3.

Please amend claim 4 as follows:

4(currently amended). A circuit as claimed in claim [3]1, wherein the change in voltage is on the gain-control terminal of the first capacitor and results in a reduction in the capacitance of the first capacitor.

Please amend claim 5 as follows:

5(currently amended). A circuit as claimed in claim [3]1, wherein the voltage on the gain-control terminal of each of the first and second capacitors is changed.

Please amend claim 9 as follows:

9(currently amended). A circuit as claimed in claim [3]1, wherein the input switch is controlled by the voltage on the gain-control terminal of the first capacitor.

Please cancel claim 27.

Allowable Subject Matter

Claims 1 and 4-26 are allowed.

The following is an examiner's statement of reasons for allowance:

Miyake et al. (6,788,108 B2) an input to which an input voltage is provided (In and Inb), a capacitor arrangement (2154, 2155), and a switching arrangement (2151) (Miyake, figure 21); wherein: the capacitor arrangement includes: a first capacitor (2154) that is configured as a voltage-dependent capacitor having a first voltage-dependent capacitance, and a second capacitor (2155), coupled to the first capacitor, that is configured as a voltage-dependent

capacitor having a second voltage-dependent capacitance. Here Miyake teaches the two transistors connected in a way to make them voltage dependent capacitors. the circuit is operable in two modes, a first mode in which the input voltage is provided to an input terminal of at least the first capacitor, and a second mode in which the switching arrangement causes charge to be redistributed between the first and second capacitors (Miyake, figure 21). Here Miyake teaches a switch 2151 which is controlled by VDD. When the switch is on, it is in the first mode and with the switch is off it is in the second mode; and the switching arrangement is configured to receive a first gain-control signal that is arranged to change the capacitance of the first capacitor and a second gain- control signal that is arranged to change the capacitance of the second capacitor (Miyake, figure 21). Here Miyake teaches the source and drain connected to switches 2152 and 2153 and if those switches get turned off, the capacitance of the capacitors will change.

Miyake does not teach wherein the switching arrangement includes an input switch for selectively coupling the input voltage to the capacitor arrangement, and wherein in the first mode, the input switch couples the input voltage to the capacitor arrangement, and in the second mode, the input switch isolates the input voltage from the capacitor arrangement; and wherein in the second mode, at least one of the first and second gain-control signals change a voltage on a gain-control terminal of the first and/or second capacitor.

Therefore, the claims are allowable

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Morris whose telephone number is (571)270-7171. The examiner can normally be reached on Monday-Friday, 7am-3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Amr Awad/
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